IN THE CLAIMS

1-20 (Canceled)

21. (Previously amended) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate, the first layer having a first surface potential;

a second layer formed on the first layer, the second layer lining the contact vias, the second layer being patterned, the second layer having a second surface potential; and

a metallization layer on the second layer, wherein the first layer and the second layer are selected to provide a desired difference between the first surface potential and the second surface potential such that the metallization layer is capable of being selectively electro-deposited on the second layer without being deposited on the first layer using a bipolar modulated voltage.

22. (Previously amended) The integrated circuit of claim 21, wherein the metallization layer comprises non-alloy copper.

23. (Previously amended) The integrated circuit of claim 21, wherein the metallization layer fills the contact vias.

24. (Previously amended) The integrated circuit of claim 21, wherein the first surface potential is lower than the second surface potential.

25. (Previously amended) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having a first surface voltage;

a second layer of material formed on the first layer, the second layer being patterned, the second layer having a second surface voltage, the second surface voltage being different than the first surface voltage; and

a metallization layer formed on the second layer, wherein the metallization layer is capable of being selectively electro-deposited on the second layer without being deposited on the first layer using a bipolar modulated voltage because of the first surface voltage and the second surface voltage.

26. (Previously added) The integrated circuit of claim 25, wherein the metallization layer comprises non-alloy copper.

27. (Previously amended) The integrated circuit of claim 25, wherein the first layer comprises polysilicon and the second layer comprises titanium nitride.

28. (Previously added) The integrated circuit of claim 25, wherein the first surface voltage is lower than the second surface voltage.

29. (Currently Amended) An integrated circuit ~~during a process of formation of the integrated circuit~~, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer of material having an exposed surface for an applied first voltage;

an insulator layer formed on the first layer, the insulator layer and the first layer having contact vias;

a second layer formed on the first layer, the second layer lining the contact vias, the second layer of material having an exposed surface for an applied second voltage, wherein the applied second voltage and the applied first voltage provide a potential difference ~~betwen~~ between the first layer of material and the second layer of material; and

a metallization layer on the second layer selectively electro-deposited on the second layer and not on the first layer using a bipolar modulated voltage because of the potential difference between the applied first voltage and the applied second voltage.

30. (Previously added) The integrated circuit of claim 29, wherein the metallization layer on the second layer fills the contact vias.

31-90 (Canceled)

91. (Previously amended) An integrated circuit, comprising:

a substrate;

a borophosphosilicate glass (BPSG) layer formed on the substrate;

a first layer of material formed on the BPSG layer, the first layer having contact vias extending through the BPSG layer to the substrate, the first layer having a first surface potential;

a second layer formed on the first layer, the second layer being patterned, the second layer having a second surface potential different than the first surface potential, the second layer lining the contact vias; and

a metallization layer formed on the second layer selectively electro-deposited on the second layer and not on the first layer using a bipolar modulated voltage because of the first surface voltage and the second surface voltage.

92. (Previously added) The integrated circuit of claim 91, wherein the first layer of material includes doped polysilicon.

93. (Previously added) The integrated circuit of claim 91, wherein the first layer of material includes undoped polysilicon.

94. (Previously added) The integrated circuit of claim 91, wherein the first layer of material includes germanium.

95. (Previously added) The integrated circuit of claim 91, wherein the second layer includes titanium nitride.

96. (Previously added) The integrated circuit of claim 91, wherein the second layer includes a barrier layer material.

97. (Previously added) The integrated circuit of claim 91, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

98. (Previously added) The integrated circuit of claim 91, wherein the metallization layer fills the contact vias.

99. (Previously amended) The integrated circuit of claim 91, wherein the first surface voltage is lower than the second surface voltage.

100. (Currently amended) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having a number of contact vias extending through to the substrate, the first layer having an innate first surface potential;

a second layer formed on the first layer, the second layer lining the contact vias, the second layer having an innate second surface potential;

a metallization layer on the second layer; and

wherein the integrated circuit is formed by a method, comprising ~~including~~:

forming the first layer of material on the substrate;

forming the number of contact vias in the first layer that extend to the substrate;

forming a second layer of material on the first layer of material such that the second layer of material lines the number of contact vias;

selectively removing portions of the second layer such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias; and

selectively electro-depositing the metallization layer on the second layer using a bipolar modulated voltage appropriate for the first surface potential of the first layer of material and the second surface potential of the second layer of material.

101. (Previously added) The integrated circuit of claim 100, wherein the metallization layer includes copper.

102. (Previously added) The integrated circuit of claim 100, wherein the bipolar modulated voltage as a first duty cycle and a second duty cycle, and the method of forming the integrated circuit includes depositing metal ions on the second layer of material during the first duty cycle, and removing any metal ions from the first layer of material during the second duty cycle that were deposited on the first layer of material during the first duty cycle.

103. (Previously added) The integrated circuit of claim 100, wherein the substrate includes borophosphosilicate glass (BPSG).

104. (Previously added) The integrated circuit of claim 100, wherein the first layer of material includes polysilicon.

105. (Previously added) The integrated circuit of claim 100, wherein the second layer of material includes a barrier layer material.

106. (Previously added) The integrated circuit of claim 100, wherein the metallization layer includes copper.

107. (Currently amended) The integrated circuit of claim 100, wherein:

the substrate includes borophosphosilicate glass (BPSG);

the first layer of material includes polysilicon;

the second layer of material includes titanium nitride; and

the metallization layer includes copper.

108. (Currently amended) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having a number of contact vias extending through to the substrate;

an insulator layer formed on the first layer;

a second layer formed on the insulator layer, the second layer lining the contact vias;

a metallization layer on the second layer; and

wherein the integrated circuit is formed by a method, comprising ~~including~~:

forming the first layer of material on the substrate and an insulator layer on the first layer of material;

forming the number of contact vias in the insulator layer and the first layer that extend to the substrate;

forming a second layer of material on the first layer of material;

selectively removing portions of the second layer such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias;

applying a first surface potential to the first layer of material and a second surface potential to the second layer of material; and

selectively electro-depositing the metallization layer on the second layer using a bipolar modulated voltage appropriate for the first surface potential of the first layer of material and the second surface potential of the second layer of material.

109. (Previously added) The integrated circuit of claim 108, wherein the metallization layer includes copper.

110. (Previously added) The integrated circuit of claim 108, wherein the bipolar modulated voltage as a first duty cycle and a second duty cycle, and the method of forming the integrated circuit includes depositing metal ions on the second layer of material during the first duty cycle, and removing any metal ions from the first layer of material during the second duty cycle that were deposited on the first layer of material during the first duty cycle.

111. (Previously added) The integrated circuit of claim 108, wherein the substrate includes borophosphosilicate glass (BPSG).

112. (Previously added) The integrated circuit of claim 108, wherein the first layer of material includes polysilicon.

113. (Previously added) The integrated circuit of claim 108, wherein the second layer of material includes a barrier layer material.

114. (Previously added) The integrated circuit of claim 108, wherein the metallization layer includes copper.

115. (Currently amended) The integrated circuit of claim 108, wherein:
the substrate includes borophosphosilicate glass (BPSG);
the first layer of material includes polysilicon;
the second layer of material includes titanium nitride; and
the metallization layer includes copper.

116. (Currently amended) An integrated circuit, comprising: ~~during a process of formation of the integrated circuit, including:~~

a substrate;

a first layer of material having a first surface potential and a number of vias extending to the substrate;

a second layer of material having a second surface potential deposited on the first layer of material, the second surface potential and the first surface potential having a predetermined potential difference, the second layer lining the contact vias, the second layer of material being patterned;

a metallization layer selectively deposited on the second layer of material using a bipolar modulated voltage having a first duty cycle and a second duty cycle such that, due to the bipolar modulated voltage and the predetermined potential difference between the first surface potential and the second surface potential, metal ions are deposited on the first layer of material and the second layer of material during the first duty cycle and metal ions ~~that were deposited on the first layer of material during the first duty cycle~~ are removed from the first layer of material and remain on the second layer of material during second duty cycle.

117. (Previously added) The integrated circuit of claim 116, wherein the first surface potential includes an innate first surface potential and the second surface potential includes an innate second surface potential.

118. (Previously added) The integrated circuit of claim 116, wherein the first surface potential includes an applied first surface potential and the second surface potential includes an applied second surface potential.

119. (Previously added) The integrated circuit of claim 116, wherein the substrate includes borophosphosilicate glass (BPSG).

120. (Previously added) The integrated circuit of claim 116, wherein the first layer of material includes polysilicon.

121. (Previously added) The integrated circuit of claim 116, wherein the second layer of material includes a barrier layer material.

122. (Previously added) The integrated circuit of claim 116, wherein the metallization layer includes copper.

123. (Currently amended) The integrated circuit of claim 116, wherein:
the substrate includes borophosphosilicate glass (BPSG);
the first layer of material includes polysilicon;
the second layer of material includes titanium nitride; and
the metallization layer includes copper.

124. (Currently Amended) An integrated circuit, comprising:
a substrate;
a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate, the first layer having a first surface voltage;
a second layer formed on the first layer, the second layer lining the contact vias, the second layer having a second surface voltage, the second surface voltage and the first surface voltage having a predetermined difference; and
a metallization layer selectively formed on the second layer using a bipolar modulated voltage having a first duty cycle and a second duty cycle, wherein:
the first duty cycle has a predetermined potential with respect to the first surface voltage and the second surface voltage such that metal ions are deposited on both the first layer and the second layer during the first duty cycle; and
the second duty cycle has a predetermined potential with respect to the first surface voltage and the second surface voltage such that metal ions are removed from the first layer and remain on the second layer during the second duty cycle.

125. (Previously added) The integrated circuit of claim 124, wherein the metallization layer includes a copper metallization layer.

126. (Previously added) The integrated circuit of claim 125, wherein the first layer of material includes doped polysilicon.

127. (Previously added) The integrated circuit of claim 125, wherein the first layer of material includes undoped polysilicon.

128. (Previously added) The integrated circuit of claim 125, wherein the first layer of material includes germanium.

129. (Previously added) The integrated circuit of claim 125, wherein the second layer includes titanium nitride.

130. (Previously added) The integrated circuit of claim 125, wherein the second layer includes a barrier layer material.

131. (Previously added) The integrated circuit of claim 125, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

132. (Previously added) The integrated circuit of claim 125, wherein the copper metallization layer fills the contact vias.

133. (Previously added) The integrated circuit of claim 125, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

134. (Previously added) The integrated circuit of claim 124, wherein the metallization layer includes a nickel metallization layer.

135. (Previously added) The integrated circuit of claim 134, wherein the first layer of material includes doped polysilicon.

136. (Previously added) The integrated circuit of claim 134, wherein the first layer of material includes undoped polysilicon.

137. (Previously added) The integrated circuit of claim 134, wherein the first layer of material includes germanium.

138. (Previously added) The integrated circuit of claim 134, wherein the second layer includes titanium nitride.

139. (Previously added) The integrated circuit of claim 134, wherein the second layer includes a barrier layer material.

140. (Previously added) The integrated circuit of claim 134, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

141. (Previously added) The integrated circuit of claim 134, wherein the nickel metallization layer fills the contact vias.

142. (Previously added) The integrated circuit of claim 134, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

143. (Previously added) The integrated circuit of claim 124, wherein the metallization layer includes a palladium metallization layer.

144. (Previously added) The integrated circuit of claim 143, wherein the first layer of material includes doped polysilicon.

145. (Previously added) The integrated circuit of claim 143, wherein the first layer of material includes undoped polysilicon.

146. (Previously added) The integrated circuit of claim 143, wherein the first layer of material includes germanium.

147. (Previously added) The integrated circuit of claim 143, wherein the second layer includes titanium nitride.

148. (Previously added) The integrated circuit of claim 143, wherein the second layer includes a barrier layer material.

149. (Previously added) The integrated circuit of claim 143, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

150. (Previously added) The integrated circuit of claim 143, wherein the palladium metallization layer fills the contact vias.

151. (Previously added) The integrated circuit of claim 143, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

CONCLUSION

Claims 29, 100, 107-108, 115-116, 123 and 124 have been amended. Claims 21-30 and 91-151 are therefor now pending. The Examiner is invited to contact the below-assigned attorney with any questions regarding the present application.

Respectfully Submitted,

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